REMARKS

Applicants respectfully request that the above-identified application be reconsidered. Claims 1-4 and 16 are pending.

An Office Action mailed June 13, 2007 (hereinafter "Office Action"), rejected Claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,784,630, issued to Saito et al. The Office Action allowed Claim 16.

Applicants have amended the specification to correct minor clerical errors. Applicants have amended Claim 1 to further clarify claim language and distinguish Claim 1 over the teachings of the cited and applied reference.

Amendments to Specification

As noted above, the specification has been amended to correct minor clerical errors.

Rejection of Claims 1-4 Under 35 U.S.C. § 103(a)

As noted above, Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Saito et al. Applicants respectfully submit that amended independent Claim 1 is allowable for the reasons set forth below.

Amended independent Claim 1 recites, *inter alia*:

> . . . wherein a number of memory banks connected to the data port is larger than a number of memory banks connected to the instruction ports, and **all the memory banks are accessible from either the instruction ports or the data ports**. (Emphasis added.)

Saito et al. does not disclose that *all the memory banks are accessible from either the instruction ports or the data ports*, as recited in amended independent Claim 1. Saito et al. does not disclose that all the memory banks are accessible from either the instruction ports or the data ports. Saito et al. discloses a multi processing system and cache memory structure in Figure 2, including an instruction cache b1 and a data cache b2 distinct and separate from each other. (Saito et al., Col. 9, line 62-Col. 10, line 5.) Because of the hardware structure shown in Figure 2 of Saito et al., those skilled in the art will appreciate that instruction cache b1 and data cache b2 cannot share any memory banks that may be included in the instruction cache b1 and data

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cache b2. Figure 2 clearly indicates that instruction cache b1 and data cache b2 have separate physical structures and separate functions, as indicated by Figure 2 and the corresponding description. This is in contrast to amended Claim 1 which recites "all the memory banks are accessible from either the *instruction ports* or the *data ports*". (Emphasis added.) In other words, any memory banks included in the instruction cache b1 or data cache b2 shown in Figure 2 of Saito et al. *can only function as either an instruction cache or data cache*, respectively, *but not both*. In contrast, *all the memory banks*, recited in Claim 1, may be accessed from either the instruction port or the data port and, thus, each memory bank, regardless of whether the memory bank is included in the instruction cache or data cache, may be used for either function of providing instructions or data. This configuration results in a more effective utilization of available memory banks. Therefore, amended independent Claim 1 is submitted to be allowable for at least the reasons discussed above.

Claims 2-4 depend from amended Claim 1 and are submitted to be allowable for at least the same reasons discussed above with respect to Claim 1.

CONCLUSION

Applicants respectfully submit that all the pending claims in this application are clearly allowable in view of the disclosures of Saito et al. Accordingly, applicants respectfully request that this application be reconsidered, the claims pending in this application be allowed, and this application be passed to issue at an early date. If the Examiner has any questions, the Examiner is invited to contact the applicants' attorney at the number set forth below.

Respectfully submitted,

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